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For: Repatterned Integrated Circuit Chip Package

1. A repatterned integrated circuit chip package comprising: first and second power supply terminals; first and second input terminals; first and second output terminals; first and second gain resistor terminals; and a plurality of connection pins on said package for interconnecting with said terminals; said first and second power supply terminals being connected to pins which are equally spaced from the pins to which said first and second gain resistor terminals are connected for balancing the effect of the package capacitance and reducing the common mode error with frequency.

2. The repatterned integrated circuit chip package of claim 1 in which one of said output terminals and one of said power supply terminals are connected together and to a single pin.

3. A repatterned integrated circuit chip package comprising: first and second power supply terminals, first and second input terminals; first and second output terminals; first and second gain resistor terminals; and a plurality of connection pins on said package for interconnecting with said terminals; said first and second power supply terminals being connected to pins which are equally spaced from the pins to which are connected said first and second gain resistor terminals with at least one other of said pins between them, respectively, for reducing package capacitance and reducing the common mode error with frequency.

4. The repatterned integrated circuit chip package of claim 3 in which one of said output terminals and one of said power supply terminals are connected together and to a single pin.

5. A repatterned integrated circuit chip package comprising: first and second power supply terminals; first and second input terminals; first and second output terminals; and first and second gain resistor terminals; a plurality of connection pins on said package for interconnecting with said terminals; said first and second power supply terminals, input terminals and output terminals being connected to selected ones of said pins, said first and second gain resistor terminals being unattached to any pins for reducing package capacitance and common mode error with frequency.

6. The repatterned integrated circuit chip package of claim 5 in which one of said output terminals and one of said power supply terminals are connected together and to a single pin.

7. A repatterned integrated circuit chip package comprising: first and second power supply terminals; first and second input terminals; first and second output terminals; first and second gain resistor terminals; a plurality of connection pins on said package for interconnecting with said terminals; and a compensating capacitor connected to one of said gain resistor terminals to balance the effect of the package capacitance on the other and reduce the common mode error with frequency.

8. The repatterned integrated circuit chip package of claim 7 in which one of said output terminals and one of said power supply terminals are connected together and to a single pin.

9. A repatterned integrated circuit chip package comprising: first and second power supply terminals; first and second input terminals; first and second output terminals; first and second gain resistor terminals; a plurality of connection pins on said package for interconnecting with said terminals; said first and second power supply terminals being connected to pins which are equally spaced from the pins to which are connected said first and second gain resistor terminals with at least one other of said pins between them, respectively; and wherein each of said at least one other of said pins is driven by a buffer amplifier to maintain each of said at least one other of said pins at the same voltage as the voltage on the pins to which said first and second gain resistor terminals are connected for balancing the effect of the package capacitance and reducing the common mode error with frequency.

10. The repatterned integrated circuit chip package of claim 9 in which one of said output terminals and one of said power supply terminals are connected together and to a single pin.